Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A magnetic memory device, comprising:

at least three terminals including first, second, and third terminals;

a spin transfer (ST) driven element including a first free layer, the ST driven element disposed between the first terminal and the second terminal; and

a readout element including a second free layer, the readout element disposed between the second terminal and the third terminal,

wherein magnetization direction of the second free layer in the readout element indicates a data state, and

wherein a magnetization reversal of the first free layer within the ST driven element magnetostatically causes a magnetization reversal of the second free layer in the readout element, thereby recording the data state.

2. (Original) A magnetic memory device as defined in claim 1, wherein the ST driven element includes a spin valve (SV).

3. (Original) A magnetic memory device as defined in claim 2, wherein the SV is a current perpendicular to the plane (CPP) spin valve.

4. (Original) A magnetic memory device as defined in claim 2, wherein the spin valve comprises:

an anti-ferromagnetic (AFM) layer;

a pinned layer;

a conductor layer; and

the first free layer.

5. (Currently Amended) A magnetic memory device as defined in claim [[5]]4, wherein the pinned layer is synthetic and includes:

a first pinned sub-layer;

a second pinned sub-layer;

a Ru layer sandwiched between the first and second pinned sub-layers, wherein the Ru layer promotes anti-ferromagnetic exchange coupling between the first and second pinned sub-layers.

6. (Original) A magnetic memory device as defined in claim 1, wherein the ST driven element includes a dual spin valve.

7. (Original) A magnetic memory device as defined in claim 6, wherein the dual spin valve comprises:

a first anti-ferromagnetic (AFM) layer;

a first pinned layer;

a first conductor layer;

the first free layer;

a second conductor layer;

a second pinned layer; and

a second anti-ferromagnetic (AFM) layer.

8. (Currently Amended) A magnetic memory device as defined in claim [[8]]7, wherein the second pinned layer is synthetic and includes:

a first pinned sub-layer;

a second pinned sub-layer;

a Ru layer sandwiched between the first and second pinned sub-layers, wherein the Ru layer sandwiched between the first and second pinned sub-layers, wherein the Ru layer promotes anti-ferromagnetic exchange coupling between the first and second pinned sub-layers.

9. (Original) A magnetic memory device as defined in claim 1, wherein the readout element includes a magnetic tunnel junction (MTJ).

10. (Original) A magnetic memory device as defined in claim 9, wherein the MTJ comprises:

an anti-ferromagnetic (AFM) layer;

a pinned layer;

an insulating barrier layer; and

the second free layer.

11. (Original) A magnetic memory device as defined in claim 1, wherein the readout element includes a dual magnetic tunnel junction (MTJ).

12. (Original) A magnetic memory device as defined in claim 11, wherein the dual MTJ comprises:

a first anti-ferromagnetic (AFM) layer;

a first pinned layer;

a first insulating barrier layer;

the second free layer;

a second insulating barrier layer;

a second pinned layer; and

a second anti-ferromagnetic (AFM) layer.

13. (Original) A magnetic memory device as defined in claim 1, wherein the readout element includes a magnetic tunnel junction (MTJ)/spin valve (SV) combination.

14. (Original) A magnetic memory device as defined in claim 13, wherein the MTJ/SV combination comprises:

a first anti-ferromagnetic (AFM) layer;

a first pinned layer;

an insulating barrier layer;

the second free layer;

a conductor layer;

a second pinned layer; and

a second anti-ferromagnetic (AFM) layer.

15. (Original) A magnetic memory device as defined in claim 14, wherein the second pinned layer is synthetic and includes:

a first pinned sub-layer;

a second pinned sub-layer;

a Ru layer sandwiched between the first and second pinned sub-layers,

wherein the Ru layer promotes anti-ferromagnetic exchange coupling between the first and second pinned sub-layers.

16. (Original) An array of magnetic memory devices for reading and writing data states, comprising:

a plurality of word lines;

a plurality of bit lines; and

a plurality of magnetic memory elements, each magnetic memory element comprising:

at least three terminals including first, second, and third terminals;

a spin transfer (ST) driven element including a first free layer, the ST driven element disposed between the first terminal and the second terminal;

a readout element including a second free layer and an insulating barrier layer, the readout element disposed between the second terminal and the third terminal; and

at least one isolation circuitry configured to select a desired magnetic memory element within the array, and to isolate the insulating barrier layer during a write operation,

wherein the readout element, the word line, and the bit line cooperate to enable a magnetization direction of the second free layer in the readout element to indicate a data state, and

wherein the ST driven element, the word line, and the bit line cooperate to enable a magnetization reversal of the first free layer within the ST driven element magnetostatically causing a magnetization reversal of the second free layer in the readout element thereby recording a data state.

17. (Original) An array of magnetic memory devices as defined in claim 16, wherein said at least one isolation circuitry comprises:

a first gate, a first source, and a first drain; and

a second transistor having a second gate, a second source, and a second drain.

18. (Original) An array of magnetic memory devices as defined in claim 17, wherein said at least one isolation circuitry and said at least three terminals are configured such that

the first terminal is coupled to the bit line,

the second terminal is coupled to the first drain,

the third terminal is coupled to the second rain, and

the first and second sources are coupled to the ground line.

19. (Original) An array of magnetic memory devices as defined in claim 18, wherein the first and second transistors are configured such that

during the write operation, current flows from the bit line through the ST driven element, through the first transistor, and into the ground line, and

during the read operation, current flows from the bit line through the readout element, through the ST driven element, through the second transistor, and into the ground line.

20. (Original) An array of magnetic memory devices as defined in claim 17, wherein said at least one isolation circuitry and said at least three terminals are configured such that

the first terminal is coupled to the first drain,

the second terminal is coupled to the bit line,

the third terminal is coupled to the second drain, and

the first and second sources are coupled to the ground line.

21. (Original) An array of magnetic memory devices as defined in claim 20, wherein the first and second transistors are configured such that

during the write operation, current flows from the bit line through the ST driven element, through the first transistor, and into the ground line, and

during the read operation, current flows from the bit line through the readout element, through the second transistor, and into the ground line.

22. (Original) A method for reading and writing a data state fro a magnetic memory device, comprising:

providing at least three terminals including first, second, and third terminals;

providing a spin transfer (ST) driven element including a first free layer, the ST driven element disposed between the first terminal and the second terminal;

providing a readout element including a second free layer, the readout element disposed between the second terminal and the third terminal;

reversing a magnetization direction of the first free layer within the ST driven element, and magnetostatically causing a magnetization reversal of the second free layer in the readout element to record a data state; and

indicating a data state by detecting a magnetization direction of the second free layer in the readout element.

23. (Original) A method as defined in claim 22, wherein reversing a magnetization direction includes applying a voltage between the second terminal and the first terminal.

24. (Original) A method as defined in claim 22, wherein indicating a data state includes applying a voltage between the third terminal and the first terminal.

25. (Original) A method as defined in claim 22, wherein indicating a data state includes applying a voltage between the third terminal and the second terminal.

26. (Original) A method for reading and writing data states for an array of magnetic memory elements, comprising:

providing a plurality of word lines;

providing a plurality of bit lines;

providing a plurality of magnetic memory elements, each magnetic memory element comprising:

at least three terminals including first, second, and third terminals;

a spin transfer (ST) driven element including a first free layer, the ST driven element disposed between the first terminal and the second terminal;

a readout element including a second free layer and an insulating barrier layer, the readout element disposed between the second terminal and the third terminal; and

at least one isolation circuitry configured to select a desired magnetic memory element within the array, and to isolate the insulating barrier layer during a write operation;

reversing a magnetization direction of the first free layer within the ST driven element, and magnetostatically causing a magnetization reversal of the second free layer in the readout element to record a data state; and

indicating a data state by detecting a magnetization direction for the second free layer in the readout element.

27. (Original) A method as defined in claim 26, wherein said at least one isolation circuitry comprises:

a first transistor having a first gate, a first source, and a first drain; and

a second transistor having a second gate, a second source, and a second drain.

28. (Original) A method as defined in claim 27, further comprising:

configuring said at least one isolation circuitry and said at least three terminals, including:

connecting the first terminal to the bit line;

connecting the second terminal to the first drain;

connecting the third terminal to the second drain; and

connecting the first and second sources to the ground line.

29. (Original) A method as defined in claim 28, further comprising:

configuring the first and second transistors, including:

directing the current to flow from the bit line through the ST driven element, through the first transistor, and into the ground line, to write the data state; and

directing current to flow from the bit line through the readout element, through the ST driven element, through the second transistor, and into the ground line, to read the data state.

30. (Original) A method as defined in claim 27, further comprising:

configuring said at least one isolation circuitry and said at least three terminals, including:

coupling the first terminal to the first drain;

coupling the second terminal to the bit line;

coupling the third terminal to the second drain; and

coupling the first and second sources to the word line.

31. (Original) A method as defined in claim 30, further comprising:

configuring the first and second transistors, including:

directing current to flow from the bit line through the ST driven element, through the first transistor, and into the ground line, to write the data state; and

directing current to flow from the bit line through the readout element, through the second transistor, and into the ground line to read the data state.